

13. (Amended) An etched optoelectronic apparatus comprising:

- AI Sub B2
- a) a semiconductor substrate having an etched pit with semiconductor sidewalls;
  - b) a dielectric layer disposed on the semiconductor substrate, wherein the dielectric layer has a hole with dielectric sidewalls, wherein the dielectric sidewalls are aligned with the semiconductor sidewalls
  - c) a patterned metal layer disposed on the dielectric layer, wherein the patterned metal layer has sidewalls aligned with the dielectric sidewalls and semiconductor sidewalls;
  - d) a patterned metal pad disposed on the dielectric layer;
  - e) solder disposed on the patterned metal pad.

14. The apparatus of claim 13 wherein the patterned metal layer has damaged portions and undamaged portions, and wherein the damaged portions are adjacent to the dielectric sidewalls and semiconductor sidewalls.

15. The apparatus of claim 14 wherein the dielectric layer is unetched in areas adjacent to the undamaged portions of the patterned metal layer.

16. The apparatus of claim 14 wherein the damaged portions of the patterned metal layer are damaged by exposure to an etching process that formed the semiconductor etched pit.

17. The apparatus of claim 13 wherein the semiconductor substrate comprises single crystal silicon and the etched pit is an anisotropically wet etched pit.

18. The apparatus of claim 13 wherein the semiconductor substrate comprises single crystal silicon and the etched pit is a directionally dry etched pit.

AI Sub C1

19. (New) The apparatus of claim 13 wherein the patterned metal layer includes a U-shaped patterned metal area, and wherein the etched pit is an anisotropically etched pit disposed inside the U-shaped patterned metal area.

20. (New) The apparatus of claim 13 wherein the patterned metal layer includes a ring-shaped patterned metal area, and wherein the etched pit is an anisotropically etched pit disposed inside the ring-shaped patterned metal area.

21. (New) The apparatus of claim 13 further comprising an optoelectronic device soldered to the patterned metal pad.

- Sub C1*
22. (New) The apparatus of claim 13 wherein the patterned metal pad is spaced away from the dielectric sidewall.
23. (New) The apparatus of claim 13 wherein the patterned metal pad and the patterned metal layer comprise identical deposited materials.
24. (New) An etched optoelectronic apparatus comprising:
- a) a semiconductor substrate having an etched pit with semiconductor sidewalls;
  - b) a dielectric layer disposed on the semiconductor substrate, wherein the dielectric layer has a hole with dielectric sidewalls, wherein the dielectric sidewalls are aligned with the semiconductor sidewalls
  - c) a patterned metal layer disposed on the dielectric layer, wherein the patterned metal layer has sidewalls aligned with the dielectric sidewalls and semiconductor sidewalls, and wherein the patterned metal layer includes a U-shaped patterned metal area, with the etched pit disposed inside the U-shaped patterned metal area;
  - d) a patterned metal pad disposed on the dielectric layer;
  - e) solder disposed on the patterned metal pad.
- Sub B3*
25. (New) The apparatus of claim 24 wherein the patterned metal layer has damaged portions and undamaged portions, and wherein the damaged portions are adjacent to the dielectric sidewalls and semiconductor sidewalls.
26. (New) The apparatus of claim 24 wherein the damaged portions of the patterned metal layer are damaged by exposure to an etching process that formed the semiconductor etched pit.
- Sub C1*
27. (New) An etched optoelectronic apparatus comprising:
- a) a semiconductor substrate having an etched pit with semiconductor sidewalls;
  - b) a dielectric layer disposed on the semiconductor substrate, wherein the dielectric layer has a hole with dielectric sidewalls, wherein the dielectric sidewalls are aligned with the semiconductor sidewalls
  - c) a patterned metal layer disposed on the dielectric layer, wherein the patterned metal layer has sidewalls aligned with the dielectric sidewalls and semiconductor sidewalls;
  - d) a patterned metal pad disposed on the dielectric layer;
  - e) solder disposed on the patterned metal pad;
  - f) an optoelectronic device on the solder.
- Sub B4*

- Sub C*
28. (New) The apparatus of claim 27 wherein the patterned metal layer has damaged portions and undamaged portions, and wherein the damaged portions are adjacent to the dielectric sidewalls and semiconductor sidewalls.
29. (New) The apparatus of claim 27 wherein the damaged portions of the patterned metal layer are damaged by exposure to an etching process that formed the semiconductor etched pit.
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